Proceedings of the ASME 2014 12th International Conference on Nanochannels, Microchannels, and Minichannels
ICNMM2014
August 3-7, 2014, Chicago, Illinois, USA

ICNMM2014-21813

ELECTRICAL INTERCONNECT AND MICROFLUIDIC COOLING WITHIN 3D ICs AND SILICON INTERPOSER

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ABSTRACT

Heat dissipation is a significant challenge for three-dimensional integrated circuits (3D IC) due to the lack of heat removal paths and increased power density. In this paper, a 3D IC system with an embedded microfluidic cooling heat sink (MFHS) is presented. In the proposed 3D IC system, high power tiers contain embedded MFHS and high-aspect ratio (23:1) through-silicon-vias (TSVs) routed through the integrated MFHS. In addition, each tier has dedicated solder-based microfluidic chip I/Os. Microfluidic cooling experiments of staggered micropin-fins with embedded TSVs are presented for the first time. Moreover, the lateral thermal gradient across a chip is analyzed with segmented heaters.

INTRODUCTION

Three-dimensional IC (3D IC) technology has been extensively explored in recent years. By significantly shortening the interconnect length as well as enabling heterogeneous integration of logic, memory, MEMS, and optoelectronics [1], 3D ICs reduce system power, system footprint and improve performance. A key challenge for high-performance 3D applications is heat removal. The reason is that both the power density of a 3D stack and the thermal resistance of the dice within the stack increase as the number of tiers increases. The latter is due to the fact that the inner dice do not have direct access to a heat sink (Fig. 1 (a)). Thus, innovative interlayer microfluidic cooling has been proposed for 3D ICs to overcome this challenge [3][4].

Due to the advancements in microfabrication, more 'complex' microstructures for improved heat sink performance have been fabricated and may outshine the performance of plain microchannels proposed in [3]. Examples of more complex microfluidic heat sink structures include enhanced microchannels [5], inline micropin-fins [6][7], staggered micropin-fins [8], and pearl chain [6] etc. Prior work in interlayer microfluidic cooling has focused on pumping a coolant into a stack through a single inlet, as shown in Fig. 1 (b) [6]. The authors demonstrated heat removal of 200 W and 400 W in a 2-tier stack and 4-tier stack, respectively in [9][10]. With this approach, it is not possible to control or tailor the flow rate in each tier. However, in a realistic 3D stack, especially in a heterogeneous stack, the power dissipation in each tier may be different (workload dependent). Thus, one needs the capability to control the coolant flow rate in each tier independently. Even more, there is likely a need to deliver the coolant to specific locations within a tier. To address this need, wafer-level batch fabricated solder microfluidic chip I/Os and fine pitch electrical microbump I/Os have been recently demonstrated [12].

Due to the integration of the microfluidic heat sink (MFHS), the chip thickness may become a few hundred micrometers, which presents great challenges to through-silicon-via (TSV) fabrication and electrical performance. Given the thickness of silicon dice with embedded microfluidic cooling, high-aspect ratio TSVs become critical in such 3D ICs and are explored in this paper.

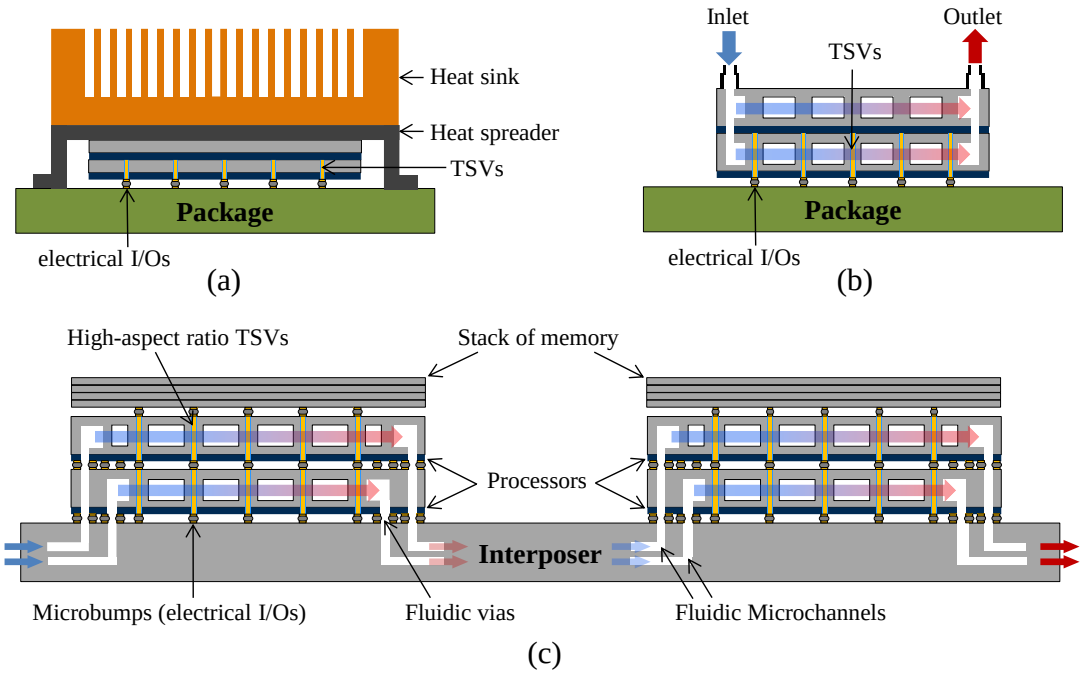

Figure 1. Schematics of (a) conventional air-cooled heat sink, (b) prior interlayer microfluidic cooling heat sink in 3D stack, and (c) the proposed 3D system featuring microfluidic delivery channels embedded within an interposer package, high-aspect ratio TSVs, and microfluidic chip I/Os

Based on a high-aspect ratio TSV technology and an innovative microfluidic chip I/O technology, this paper presents a 3D IC system featuring a silicon interposer with embedded fluidic delivery microchannels and an array of 3D stacked processor and memory tiers (Fig. 1 (c)). As shown in the figure, processor tiers may each contain an embedded MFHS with high-aspect ratio TSVs routed through the integrated MFHS. In addition, each tier has its own dedicated microfluidic chip I/Os for fluidic delivery. The coolant flow rate in each tier can be tailored independently according to the heat dissipation of each tier, i.e., tier-specific cooling. This approach helps minimize the vertical thermal gradient between tiers when each tier dissipates different power. Pumping power can also be reduced by adjusting the flow rate to the needed value for a given power dissipation per tier. The proposed local coolant delivery mechanism, which is also based on the solder chip I/O technology, may minimize the lateral thermal gradient within a single tier as well. Moreover, since the MFHS is chip-scale, this approach allows high lateral scalability of the electronic components, i.e., placing an array of 3D ICs laterally next to each other. This greatly enhances off-chip connectivity.

This paper is organized as follows: Section II describes the fabrication and electrical characterization of high-aspect ratio TSVs in a micropin-fin heat sink. In Section III, fabrication, assembly, and testing of electrical and fluidic I/Os (microbumps) are presented. Section IV describes microfluidic testing of the micropin-fin heat sink with embedded TSVs. In addition, thermal testing with four segmented heaters is also performed, followed by conclusions in section V.

HIGH-ASPECT RATIO TSVS EMBEDDED IN MICROPIN-FIN HEAT SINK

In general, embedding a microfluidic heat sink requires a die to be relatively thick since the height of the heat sink is strongly related to its cooling ability. In previous publications on microfluidic cooling [5-10], a die with embedded MFHS is approximately five times thicker than a conventional 3D IC die that ITRS projects. This not only degrades electrical performance due to increased electrical parasitics of the TSVs (capacitance), but also limits the number of TSVs between tiers because the aspect ratio of TSVs is typically limited by fabrication. Thus, we develop high-aspect ratio TSVs to allow integration within the MFHS and maintain electrical benefits. In this section, we demonstrate 13 μm diameter and 300 μm tall TSVs (aspect ratio of 23:1) embedded within micropin-fin heat sink. A four by four array of TSVs is integrated in micropin-fins with a diameter of 150 μm and a height of 270 μm. The pitch among the TSVs is 24 μm.

Fabrication

Figure 2 summarizes the overall fabrication steps. The fabrication of TSVs within micropin-fins starts with a 300 μm thick dual-side-polished silicon wafer. Silicon dioxide is deposited and patterned on the wafer as a mask during silicon etching. High-aspect ratio vias (~23:1) are etched using a Bosch process that alternates between SF_6 (etch step) and C_4F_8 (deposition step). Thermal oxide (~1 μm) is then grown in a furnace to isolate the TSVs from the substrate. Titanium and copper are deposited to form a seed layer at the back side of the

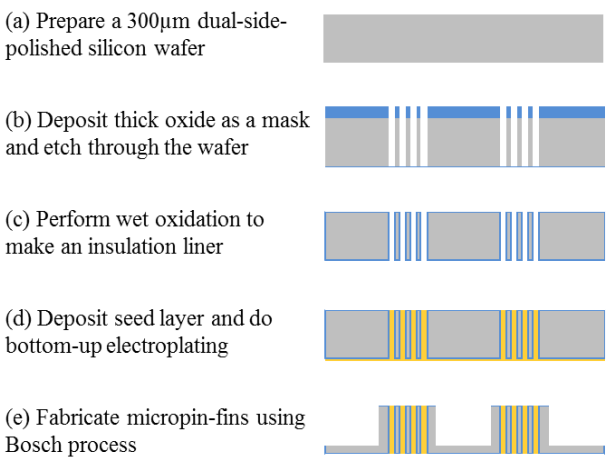

Figure 2: Fabrication process flow of high-aspect ratio TSVs within micropin-fins

wafer. Next, using DC electroplating, via holes are pinched off, and thus forming a seed layer to fill the vias with copper. Using this newly formed layer, a pulsed bottom-up electroplating is performed using Enthone DVF electroplating solution to fill the vias with copper. Over-electroplated copper (on the opposite end of the wafer) is then removed using chemical mechanical polishing (CMP). Figure 3 illustrates optical images of fully-filled TSVs (cross-section and top view). Following polishing, silicon is etched around the TSVs using the Bosch process to form 150 μm diameter and 270 μm tall micropin-fins. The fabricated TSVs are 13 μm in diameter and 300 μm deep. Angled and cross-sectional views of the fabricated TSVs within the micropin-fins are shown in Fig. 4 [13].

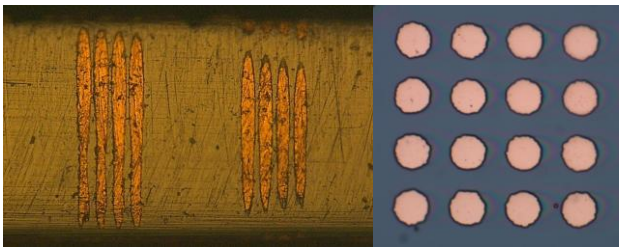

Figure 3. A 4 x 4 array of the fabricated high-aspect ratio TSVs: cross-sectional view (left) and top view (right)

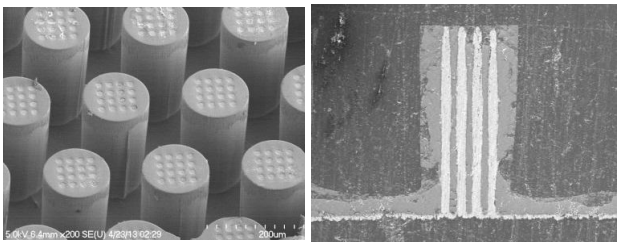

Figure 4. SEM images of micropin-fins with high-aspect ratio TSVs: angled view (left) and cross-sectional view (right)

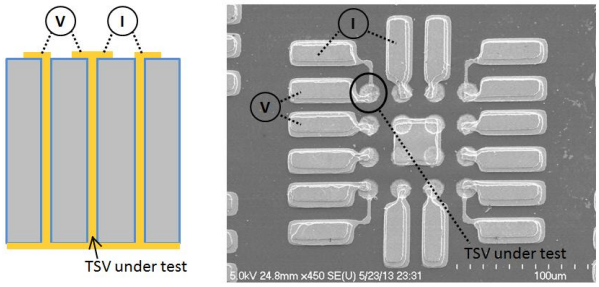

Figure 5. Electrical resistance measurements of TSVs using four-point Kelvin technique

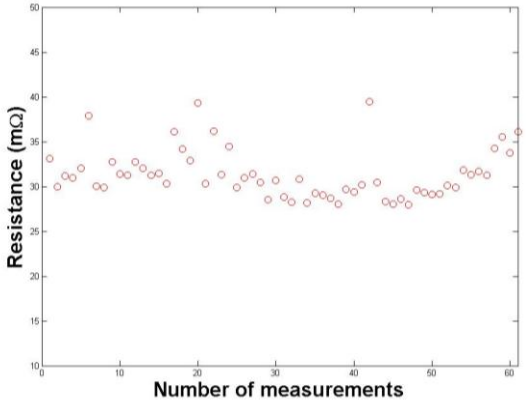

Figure 6. Electrical resistance measurement results of a TSV

Electrical Measurements

The resistance of the fabricated TSVs is measured using four-point Kelvin technique. For the resistance measurements, gold pads (50 μm × 20 μm) are deposited using an e-beam evaporator, as shown in Fig. 5. The measured average value for 61 measurements (Fig. 6) is 31.33 mΩ with 2.72 mΩ standard deviation. The theoretical TSV resistance is 32.7 mΩ and matches the experimental results well.

ELECTRICAL AND FLUIDIC I/O FABRICATION, ASSEMBLY, AND TEST

Fabrication and Assembly

The fabrication process of the silicon die with electrical and fluidic microbumps and embedded micropin-fin heat sink is illustrated in Fig. 7. As previously noted, the process begins with a 300 μm thick dual-side-polished silicon wafer. A silicon dioxide layer of 3 μm is deposited on one side of the wafer using plasma-enhanced chemical vapor deposition (PECVD). Next, fluidic vias and micropin-fins are etched on the other side of the wafer using two Bosch etch steps. The fluidic vias are halfway etched (~100 μm deep etch) during the first etch step. In the second etch step, the vias are etched through (additional ~200 μm of depth) while simultaneously etching the micropin-fins. Following the silicon etching steps, a titanium/copper (25 nm/250 nm) layer is sputtered on the silicon dioxide as a seed

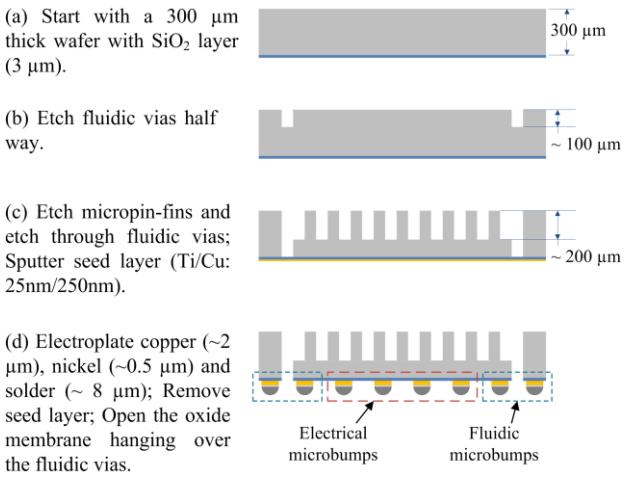

Figure 7. Fabrication process flow of microbumps with fluidic heat sink

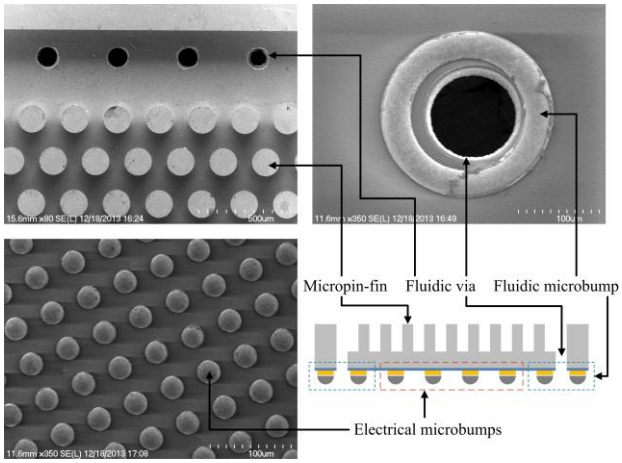

Figure 8. SEM images of the fabricated micropin-fins, electrical microbumps, fluidic microbumps, and fluidic vias

layer for electroplating. Next, copper pads for electrical and fluidic microbumps and fine-pitch interconnects are electroplated followed by electroplating of nickel and solder on the pads. After electroplating copper, nickel, and solder, the seed layer is removed and the oxide membrane suspended over the fluidic vias is opened. Figure 8 illustrates the fabricated electrical and fluidic microbumps, micropin-fins and fluidic vias. After fabrication, the silicon die is flip-chip bonded onto a silicon interposer using a Finetech flip chip bonder, which provides sub-micron alignment accuracy.

Verification by Electrical and Fluidic Tests

Following assembly, electrical and fluidic tests are conducted to verify the bonding and the sealing quality. The resistance of a single electrical microbump is measured using four-point Kelvin technique. Figure 9 illustrates the resistance of eight electrical microbumps. The average resistance is

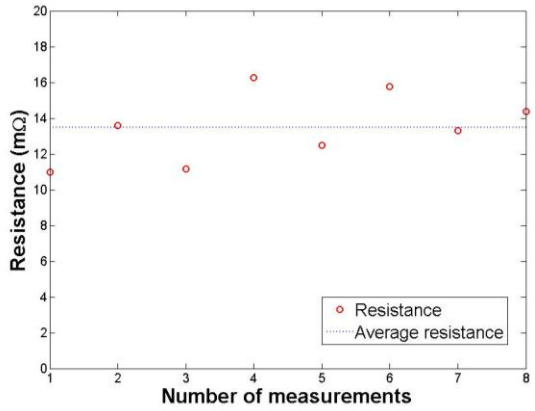

Figure 9. Electrical resistance measurement results of an electrical microbump

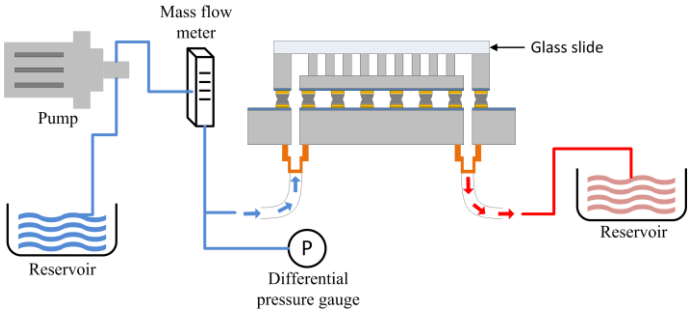

Figure 10. Capping the micropin-fin heat sink and attaching inlet/outlet ports and tubes for fluidic testing.

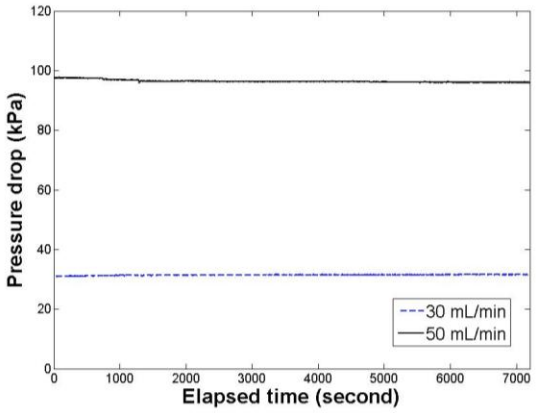

Figure 11. Fluidic test results (continuous DI water pumping for 4 hours at flow rates of 30 and 50 mL/min)

approximately 13.5 mΩ.

Next, the sealing quality of the fluidic microbumps is tested. First, the micropin-fin heat sink is capped with a glass cover (to facilitate visual inspection), as shown in Figure 10. Next, manifolds and tubes are attached to the back side of the interposer, and the pressure drop between the inlet and outlet ports is measured. During testing, DI water is pumped into the die continuously for 4 hours at flow rates of 30 and 50 mL/min.

Table 1: Die and bonding parameters

Parameter	Value
Die size	~ 1 cm by 1cm
Number of fluidic microbumps	42 (21 each row)
Number of electrical microbumps	22,500 (150 by 150)
Temperature ramp rate	2 ^{o}C/s
Peak temperature	230 ^{o}C
Peak temperature duration	15 s
Bonding force	~7 N

The measured pressure drop at each flow rate is very stable, as shown in Fig. 11. No obvious pressure drop change occurs and no leakage was visually observed, which indicates stable fluidic sealing. The bonding profile and die parameters of the assembled test chip are summarized in Table I.

MICROFLUIDIC TESTING OF MICROPIN-FIN ARRAY

Staggered cylindrical micropin-fin array has been widely explored as a microfluidic heat sink due to its large surface area and high convective heat transfer relative to other heat sink designs. The critical dimensions of micropin-fins are shown in Fig. 12; diameter (D), transverse pitch (P_T), and lateral pitch (P_L) are shown, respectively.

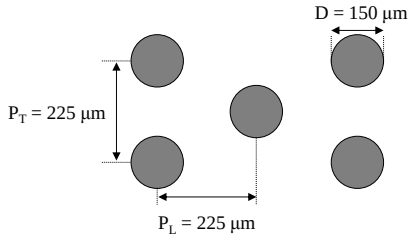

Figure 12. Layout of the staggered micropin-fin array; Diameter (D), transverse pitch (P_T), and lateral pitch (P_L) are shown.

Fluidic Testing of Micropin-fin with Embedded TSVs

Integration of TSVs into micropin-fin array was demonstrated in Section II. After capping the sample using a glass slide, platinum heater is patterned in a spiraling shape, as shown in Fig. 13, to enable thermal testing of the TSVs integrated within the micropin-fin heat sink. A power source is directly connected to the heater to supply constant power during testing. In this work, the heater also serves as a temperature detecting sensor since resistance of platinum increases linearly with temperature. By detecting change in resistance of the platinum heater, the temperature of the sample can be calculated. Figure 14 illustrates the measured on-chip temperature with DI water flow rates of 60 and 80 mL/min. The temperature of the heater increases by 23 and 20 ℃, respectively at the maximum power level of 75 W/cm^2. The calculated thermal resistance is 0.3187 and 0.2799 K/W at

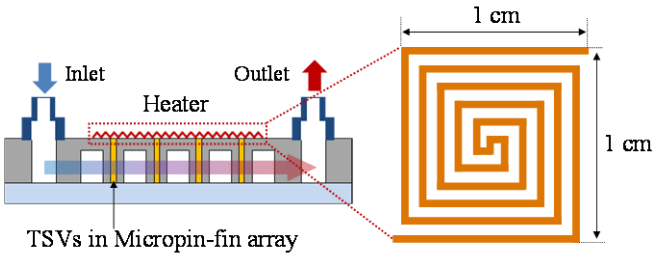

Figure 13. Microfluidic cooling testing using TSV-integrated micropin-fin array

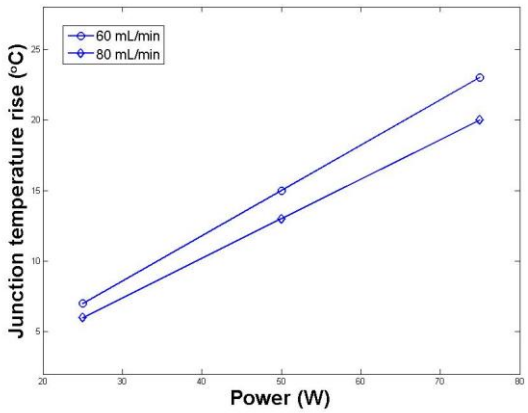

Figure 14. Junction temperature rise as a function of power dissipation for micropin-fin with integrated TSVs

60 and 80 mL/min, respectively. Power densities from 25 to 75 W/cm^2 were used in this experiment. To isolate the heat dissipation from the ambient, a thick epoxy layer was deposited on top of the heater. The energy removed by the fluid can then be calculated using the inlet and outlet temperatures. The error between applied power and power removed by the fluid is within 10 %.

Fluidic Testing for Lateral Thermal-gradient Detection

We have previously reported thermal measurements of a 2-tier testbed with MFHS in each tier [14]. It is known that coolant temperature increases as it flows through the MFHS, and thus the chip temperature will increase along fluid flow. To capture the lateral temperature increase due to this effect, a single tier measurement with uniform power density is performed with four segmented heaters along the flow direction, as shown in Fig. 15. Each heater has dimensions of 1 cm × 0.22 cm. Figure 16 illustrates the temperature of each heater on the chip as the total chip power density ramps from 25 to 100 W/cm^2 (the DI water flow rate is kept at 80 mL/min). In the high power density case (100 W/cm^2), the junction temperature of heater 4 (i.e., the heater closest to the outlet) increases by 33 ℃ while that of heater 1 increases by only 17 ℃. This result is expected since the coolant temperature increases as it flows from the inlet to the outlet, and thus, the chip junction temperature also increases. The average junction-to-inlet

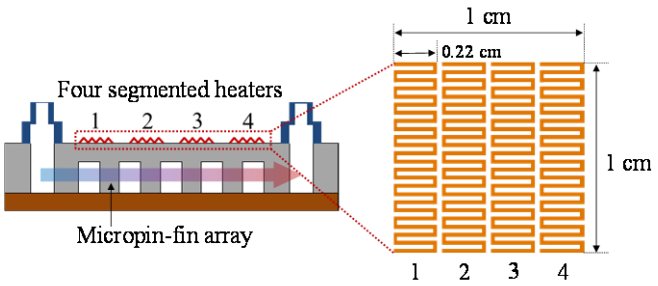

Figure 15. Microfluidic cooling testing with segmented heaters for lateral thermal-gradient detection

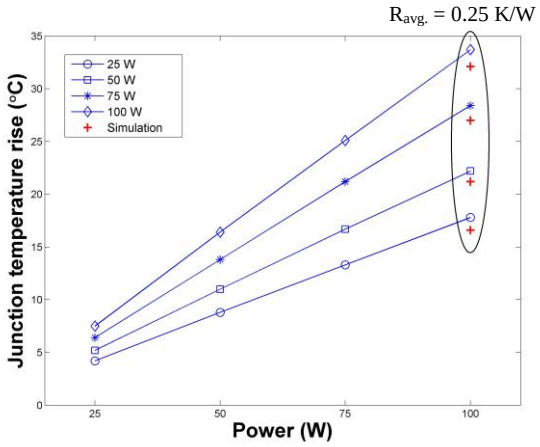

Figure 16. Junction temperature rise as a function of power dissipation for different heater locations along the flow direction. ANSYS simulation for the 100 W case is also plotted as a validation.

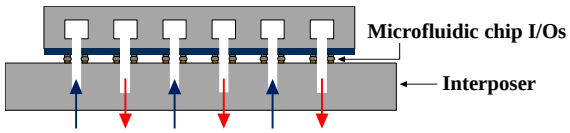

Figure 17. 3-D stack with multiple microfluidic chip I/Os for localized coolant delivery

thermal resistance of the heat sink is 0.25 K /W, resulting in an average heat transfer coefficient (h_{avg}) of 3.8 × 10^4 W/(m^2 K). The maximum error in the energy difference between injected power and power consumed by the fluid is around 10 %. The chip design is simulated using ANSYS Fluent at a power density of 100 W/cm^2. Average junction temperature for each case is extracted from the simulation results and plotted in Fig. 16. The difference between the experimental results and the simulations is less than 1.6 ℃. The figure also illustrates that the lateral thermal gradient across the chip becomes exacerbated as the power density increases.

One way to mitigate the thermal gradient is to increase the flow rate. However, this will also increase both the pressure drop and the pumping power. Thus, we propose an alternative solution to mitigate the lateral thermal gradient based on local coolant delivery, as shown in Fig. 17. This system is enabled through the microfluidic chip I/Os, which deliver fresh coolant to each core, allowing the cores to work symmetrically.

CONCLUSIONS

This paper presents novel technology enablers for 3D integration, including micropin-fin heat sink with high-aspect ratio TSVs as well as fine-pitch electrical and fluidic microbumps. TSVs with an aspect ratio of 23:1 are fabricated within micropin-fins and characterized. Electrical and fluidic microbumps are fabricated, assembled, and tested. Microfluidic cooling measurements demonstrate the cooling performance of the TSV-integrated micropin-fin heat sink. The thermal gradient effect of microfluidic cooling is discussed, and a possible solution with multiple microfluidic I/Os is proposed.

ACKNOWLEDGMENTS

This work has been carried out in part under support from Semiconductor Research Corporation (SRC) contract 2011-KJ-2189 and from Defense Advanced Research Projects Agency (DARPA) contracts N66001-12-1-4240 and HR0011-13-2-0008**.** The authors also thank Enthone for providing the electroplating solution and Cabot Microelectronics Corporation for providing CMP slurries.

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